AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs as shown.

[0014] Before proceeding further, it should be apparent from the figures that the high-speed output 116 and the low-speed output 120 are a high-speed input and a low-speed input to the FSD interface 100. These inputs are also referred to herein as the first and second voltage inputs. The high-speed output 116 and the low-speed output 120 are also summed individually in a summing module 136 to provide different analog voltages each representing a particular speed. For example, the high-speed output 116 is summed into a 10KΩ resistor via a 1MΩ resistor. Meanwhile, the filtered low-speed output 126 is summed into the 10KΩ resistor via a 499KΩ resistor to generate a summed voltage. The summing module 136 thus provides a summed voltage that represents either a high-speed signal or a low-speed signal. The summed voltage is further conditioned at a filter module 148 to filter out undesirable noise or to clean the summed voltage so that the summed voltage is detectable by an A/D converter ("ADC") 140. The ADC 140 can be embedded in a micro-controller 144 as shown in FIG. 1, or the ADC 140 is external to the micro-controller 144. Examples of micro-controller include embedded micro-controller, such as PIC 16C717I/SS from MicroChip, and ST micro-controller from ST Microelectronics. The micro-controller 144 reads in the summed voltage, and then generates a software control or selection signal based on the summed voltage. The micro-controller 144 further includes an internal memory (not shown) that stores a plurality of codes and associated parameters. Although the memory is described as internal to the micro-controller 144, external memory can also be used in the interface to store data such as customer-specific parameters.